Device reliability studies using low frequency noise measurements

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Outline

• Introduction to low frequency noise
• Devices under study
• Experimental setup
• Gate electric field stress experiment
• Channel electrical field stress experiment
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Defect spectroscopy using noise

- $\frac{1}{f^\gamma}$ noise is an excellent *interface defect* quality indicator for the channel.

$$\frac{S_i}{I^2} = \frac{\alpha_H}{Nf}$$ where $\alpha_H$ is the Hooge parameter

- Lorentzian due to random telegraph noise is an excellent *point defect* probe.

![Graph showing 1/f noise, GR Lorentzian, and Thermal noise](graph.png)

$S_i$ (A²/Hz)

Frequency (Hz)

CB

Capture

Emission $E_T$

VB
Devices under study

- Commercial device
  - Gate length ($L_G \sim 0.65 \, \mu m$)
  - 10 gate finger device with 2 mm periphery.
  - Ceramic packaged.

- AFRL sample
  - Gate length ($L_G \sim 0.1 \, \mu m$)
  - 2 gate finger device with $W_G \sim 160 \, \mu m$
  - Ceramic packaged.

- Source
- Drain
- Gate (Ni/Au)
- 18nm $Al_{0.26}Ga_{0.74}N$ barrier
- 0.8µm GaN buffer
- Silicon substrate
- SiN
- Passivation
- 1.5 nm GaN cap

- Source
- Drain
- Gate
- 18nm $Al_{0.26}Ga_{0.74}N$ barrier
- 0.8µm GaN buffer
- Silicon substrate
- SiN
- Passivation
- 1.5 nm GaN cap

- Source
- Drain
- Gate
- 15nm $Al_{0.28}Ga_{0.72}N$ barrier
- 2.25µm GaN buffer
- SiC substrate
- SiN
- Passivation
- 3 nm GaN cap

- Source
- Drain
- Gate
- 15nm $Al_{0.28}Ga_{0.72}N$ barrier
- 2.25µm GaN buffer
- SiC substrate
- SiN
- Passivation
- 3 nm GaN cap

- FP extension
- Source
- Drain
- Gate (Ni/Au)
Stress measurement setup

- Simultaneous high current (~ 4A) and voltage (~ 50 V) stress capability.
- Both SMU and PSU are programmable for step/stress/recovery type methodologies.
- Fully automated for both stress and noise measurements.
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  • *Gate electric field stress experiment*
• Channel electrical field stress experiment
Gate stress experiment

- Gate stack stressed from -5V to -20V for 10 minutes each with drain and source grounded.
- Transconductance $I_G, I_D-V_G$, Drain and Gate current noise measured between each stress bias.
- Device disconnected to the bias supplies after stress. Noise and I-V measurements were continued for several weeks thereafter.
Threshold voltage ($V_T$) constant till $V_G = -10$ V and then trends positive as $V_G$ increases due to large trap filling under gate.

$V_T$ recovers to its pre-stress level subsequently by slowly becoming more negative. This is analogous to slow de-trapping of electrons beneath the gate. (Ref. Sahoo 2003)
DC transient effect

- Gate current during stress *decreases in magnitude* as a function of applied stress, can be explained by gate potential becoming more negative due to trap-filling under the gate stack during stress (Ref. Sahoo 2003).
Drain noise evolution

- Drain current noise completely recovers to its pre-stress levels as threshold voltage becomes more negative due to de-trapping of electrons.
- No channel degradation during or after the stress !!

\[
\frac{S_{I_D}}{I_D^2} \equiv \frac{S_{R_{CH}}}{R_{CH}^2} = \frac{\alpha_{CH}}{N_{CH} f}
\]

Where, \( N_{CH} = C_{AlGaN} (V_{GS} - V_T) \)

\[
\therefore V_{GS} \text{ is constant}
\]

\[
\therefore V_T \downarrow \Rightarrow N_{CH} \uparrow \Rightarrow \frac{S_{I_D}}{I_D^2} \downarrow
\]
Gate noise evolution

- Permanent degradation of the gate current noise !!
- Increase of trap density located at the gate edges.
Trap states are created at the GaN/AlGaN semiconductor interface during stress which leads to gate noise increase. Inverse piezo-electric effect is the possible explanation since not very high gate current densities (~0.038 A/mm²) are involved during stress.

• Trap levels at the $E_{F-M}$ quasi-Fermi level are likely candidates for modulating the trap assisted gate stack tunneling current.

• The DC transient effects are due to trap filling during stress and trap emptying after stress.
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• *Channel electrical field stress experiment*
## Channel stress experiment (GaN-on-Si)

<table>
<thead>
<tr>
<th>Test</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS}$ (V)</th>
<th>$P_{Dmax}$ (channel)</th>
<th>Stress time</th>
<th>Stress type</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>20</td>
<td>-1.7</td>
<td>2.3 W/mm</td>
<td>5 minutes</td>
<td>Hot carrier and self-heating</td>
</tr>
<tr>
<td>II</td>
<td>2</td>
<td>2</td>
<td>0.575 W/mm</td>
<td>30 minutes</td>
<td>Self-heating</td>
</tr>
<tr>
<td>III</td>
<td>10 to 30 step</td>
<td>-4</td>
<td>0.45 mW/mm</td>
<td>60 minutes</td>
<td>Hot-carrier</td>
</tr>
</tbody>
</table>

- Gate bias varied to control channel carriers and therefore, current.
- Transient and permanent changes observed in each stress condition.
Results
Increase of trap density at the AlGaN/GaN interface.

Hooge parameter ($\alpha_H$) changed from $\sim 10^{-3}$ to $1.5 \times 10^{-2}$
Channel stress experiment (GaN-on-SiC)

- Hot carrier and self-heating stress at constant $V_{DS} = 25V$, $V_{GS}=0V$, $T=160s$, and $P_{D_{\text{max}}} = 18.75W/mm$
- Hooge parameter ($\alpha_H$) changed from $\sim 10^{-3}$ to $8.4 \times 10^{-2}$
Conclusions

- Characterized permanent trap creation and migration in the gate stack after high electric field stress.
- Characterized permanent degradation in the AlGaN/GaN interface after high electric field and self-heating stress.